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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MERID, ARADOM B	
ART UNIT	PAPER NUMBER
2631	11

DATE MAILED: 02/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/694,806	BEN-ELI, DAVID	
	Examiner	Art Unit	
	Aradom B. Merid	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *04-23-1998*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected to because of the following informalities: the equation $S(t)= A (Cos2\pi f_c t + \theta_k + \varphi)$ given for the quaternary phase modulation transmitted signal on page 1 paragraph 3 is incorrect. It should be changed to $S(t)= A Cos(2\pi f_c t + \theta_k + \varphi)$. Appropriate correction is required.

Claim Objections

2. Claims18 and 19 are objected to because of the following informalities: Claim 18 is incorrectly dependent on claim 18. Appropriate correction is required. Examiner, however, assumes that claim 18 is dependent on claim 15.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claim recites addressing a memory by a register that is partitioned in to a precursor and postcursor registers in which the precursor register addresses a first memory portion and the postcursor register addresses the memory portion at **odd times**. The claim limitation further recites that a second memory is addressed by the precursor register and the first memory by the postcursor register by using **reversed addressing at even times**.

Examiner finds that addressing the memory portions at **odd and/ or even times** by the registers (precursor and postcursor), and memory addressing by the postcursor register using **reversed addressing** are not clearly described in the specification. Examiner also finds that the "...**high address factor**..." and "...**low address factor**..." (in claim 18) are not clearly described in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "... **said predetermined number of samples**..." line 12-13. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 recites the limitation "... wherein **the shift register**..." line 20. There is insufficient antecedent basis for this limitation in the claim. Examiner, however, assumes that phrase "**the shift register**" refers to the "**register**" as recited in claim 1.

Claim 3 is inherently rejected as depending on the rejected base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Rossiter (U.S. Patent No. 4,573,136 of record).

Based on the examiner's assumed understanding of the claimed invention, Rossiter teaches a method (or an apparatus) of addressing a memory means in a sum – of – product multiplier device that comprises a memory which is split into two sub-memories - RAM0 and RAM1, and RAM loading logic circuits (registers) **24** and **25** to address the sub-memories . Both sub-memories

which contain pre-computed digital representations are addressed by the contents of the RAM loading logic **24** and alternate loading logic **25.** That is the contents of each sub-memory location are determined by the coefficient values which are stored in the loading logic **24** and alternate logic **25** as claimed in the limitations of claim1, 10 and 14 (Fig. 4, col.5, lines 38-40, and col. 6, lines 27-40 and col.3, lines 50-62).

As to claim 2 and 3, Rossiter claims addressing pre-computed digital samples which are stored in a plurality of memories in response to applied input bits. This implies the predetermined samples stored in sub –memories (RAM0 and RAM1) are accessed by the input bits of the RAM loading logic **24** and **25** (claim1 on col. 6, lines 24-31) in which the memory address is incremented or decremented to locate the address of the predetermined samples in the sub-memories. The pre-computed digital samples, as mentioned above, are stored in the mentioned sub-memories RAM0 and RAM1 which can be thought as a Look Up Table.

Regarding to claim 4 Rossiter further describes that the amount of memory required is based on the "m" word number (where m is even) in which the "m/2" number are stored in the ram loading register **24** and the remaining "m/2" number are stored in the alternate ram loading register **25**, to access the sub-memories RAM-0 and RAM-1 with $\mathbf{2}^{m/2}$ word memories(col.4, lines 36-60).

Rossiter also teaches providing a sum of product of the input binary data and weighting coefficients stored in the sub-memories RAM0 and RAM1 by

multiplying the input binary data with the weighting coefficients and adding each product by the adder **22** to produce the sum of product as claimed in claim 6 and 7(claim1 on col.6, lines 25-45). Rossiter also teaches that the sign of the inputted binary weighted data is indicated by the first bit of the data (col. 1, lines 29-57) as claimed in claim 10 and 11 and addressing the sub-memories by the remaining bits of the RAM loading circuits as claimed in claim 12. The sub-memories RAM0 and RAM1 can be integrated in one memory as shown in Fig.2 (as claimed in claim 13).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is also rejected under 35 U.S.C. 102(b) as being anticipated Testu Sakata et al., A New Fully-Digitalized π/4-Shift QPSK Modulator for Personal Communication Terminal", IEEE, ICUPC 1994, Pages 921-926.

Based on the examiner's assumed understanding of claimed invention, Testu teaches π/4-Shift QPSK Modulator of accessing a memory by a means of the contents in I-channel shift register and Q-channel shift register in which each shift register has

one bit address and two bit address component alternately. That is each of the shift registers can have a register with a two bit at odd times and one bit at even times to access the memory . The I and Q shift registers (as the precursor and postcursor registers on the claimed invention)shown in Fig.2 (a) even symbol timing and (b) odd symbol timing (page 922) ,alternately represent the address in memory. Testu also teaches addressing a memory by reversing the bit order in one of the registers to reduce the memory capacity (page 921, Section 2.1) .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rossiter (U.S. Patent No. 4,573,136 of record) in view of Testu Sakata et al., A New Fully-Digitalized $\pi/4$-Shift QPSK Modulator for Personal Communication Terminal", IEEE, ICUPC 1994, Pages 921-926.

Based on the examiner's assumed understating of the claimed invention, Rossiter as discussed above with respect to the rejection of claims 1-7 teaches addressing precomputed samples stored in sub-memories through the binary data input stored in the RAM loading logic circuits. However, Rossiter fails to discuss the

amplitude representations of the inputted binary data in the register. Testu discusses representing the alternate symbol data in the registers I-channel and Q-channel (Fig. 2) by two bits for every even symbol and by one bit for every odd symbol in the registers to accommodate the transmission of four signals in $\pi/4$-Shift QPSK modulation and reduce memory size of the ROM (Section 2.1, pp. 921-922). Therefore implementing Testu's method of representing the amplitude of input data by two bits for every even symbols and by one bit for every odd symbol in the register in order to express the transmission of multiple signals and to reduce memory size would have been obvious to an ordinary person skilled in the art.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 14-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Rossiter (U.S. Patent No. 4,573,136 of record) in view of Misaizu (U.S. Patent 5,487,089 of record).

Based on the examiner's assumed understanding of the claim invention, Rossiter discloses an apparatus for addressing the sub-memories RAM0 and RAM1, which can be integrated in one memory as shown in Fig.2 (as claimed in claim 17), by the binary weighted data in the RAM loading logic circuits **24** and **25** (as the precursor and postcursor registers) alternately, (col.5, lines 15-34); and an adder **22** to add the output

RAM0 and RAM1 as claimed in claim 16 (Fig.4 and claim1 on col.6, lines 36-40), but fails to disclose the implementations of plurality of multiplexers to select the section of the register by which the memory can be addressed. Rossiter also fails to mention memory addressing by Most Significant Bits, and Least Significant Bits which is provided by a counter to increment and decrement the Least Significant Bits, and a converter form bits to symbol and fails to discuss a digital to analog converter to convert the digital data into analog.

Misaizu , however, discloses a plurality of selectors which function as multiplexers that receive the output signal of the register **2** and transmits the selected symbol signal to address the memory ROM as recited in claim limitations of claims 14,15 and 20 (col.4, lines 47-52). Misaizu also teaches memory addressing that uses the higher order –address to access a portion of the ROM (higher address where one of the Most Significant Bits are used to address the higher portion of the memory) while addressing a lower-order address which is provided by a counter **27** where one of the Least Significant Bits are utilized to access a lower portion of the ROM (col. 3, line 11-21) as claimed invention in claims 18-21. Misaizu, further discusses the implementation of signal conversion device **1** from bits to symbols (col.4, lines 24-34) and the implementations of a digital to analog converter for converting the output digital data from ROM into analog base band signal as claimed in claims 22 and 23 (col.4, lines 11-15).

Therefore implementing Misazu's use of plurality of selectors (multiplexers) in order to select the section of register by which a memory is addressed quickly where in

the high order-address and low order-address method of addressing is used concurrently, and adding the digital to analog converter to convert the digital data output of the accumulator and shifter in to analog base band signal in Rossiter's claimed invention in order to reduce the memory size of the ROM and to access the memory fast would have been obvious to an ordinary person skilled in the art.

Conclusion

The following references are also included because they discuss relevant issues to the claimed invention.

Hershey et, al.	U.S. Patent Number: 5,586,266
Corry	U.S. Patent Number: 5,500,811
Hershey	U.S. Patent Number: 5,586,266
Lampe et al.	U.S. Patent Number: 5,633,893
Hershey	U.S. Patent Number: 5,548,775
Deutsch	U.S. Patent Number: 4,713,997

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aradom B. Merid whose telephone number is 703-305-8953. The examiner can normally be reached on 8:00am-5:00pm (Mon. - Fri.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohamed Ghayour can be reached on 703-306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Aradom B. Merid